REMARKS

Claims 1-42 are now in this application, new claims 35-42 having been added in this paper. Claims 1-34 stand rejected and are now presented for reconsideration in view of the following remarks.

Claim 7 was "rejected under 35 USC §112, second paragraph, as being indefinite".

In explaining this rejection, the Examiner first noted that the limitation "clock receivers" in claim 7, as originally presented, lacks antecedent basis. In response to this point, claim 7 has now been amended so as to depend from claim 5, which provides clear antecedent basis for the limitation "clock receivers".

Further in regard to the rejection of claim 7 under §112, the Examiner asserted that the term "applying clock gating" was "not understood by conventional meaning". In this regard, Applicants respectfully direct the Examiner's attention to the discussion at paragraphs 5 and 34 of the specification of the present application. Specifically, one of ordinary skill in the art would readily understand on the basis of those paragraphs, that "clock gating" refers to selectively turning off a clock signal in a portion of an integrated circuit. It is therefore respectfully submitted that the rejection of claim 7 in this respect should be reconsidered and withdrawn.

Claims 1, 2 and 31 were "rejected under 35 USC §102(b) as being anticipated by the Matsumoto et al. reference (U.S. Patent 5,448,188)".

Claim 1 is directed to a "method of generating a clock signal on an integrated circuit (IC)" and recites the steps of "generating a differential sinusoidal signal pair

comprising a first sinusoidal signal and a second sinusoidal signal" and "generating a clock signal from the differential pair for the IC by employing both the first sinusoidal signal and the second sinusoidal signal to form the clock signal".

Applicants respectfully urge that the Matsumoto et al. reference has nothing to do with generating a clock signal, as recited in claim 1. As explained in columns 1 and 2 of the Matsumoto et al. reference, the general subject of the reference is circuitry for muting or mixing video signals. Moreover, the circuit of FIG. 1 of the reference, upon which the Examiner appears to rely, is for selectively muting an input signal (see column 6, lines 3-6) and not for generating a clock signal.

To go into further detail, there is not the slightest indication in the discussion of FIG. 1 of the Matsumoto et al. reference that the output signal Vout of the circuit shown in FIG. 1 is to be used as a clock signal. Rather, in a non-muting operation mode of the circuit, the signal Vout corresponds to the input signal Vin (column 5, lines 46-49) and accordingly is an information signal such as a brightness component of a video signal. When the circuit of FIG. 1 is in a muting operation mode, the output signal Vout is a constant level.[1] Thus, the output signal Vout of the circuit of FIG. 1 of the Matsumoto et al. reference is either a video signal component or a constant voltage level, neither of which is a clock signal for an integrated circuit. It follows that the Matsumoto et al.

[1] See column 5, lines 65-68, which indicates that "Vout becomes Vcc - I2 x R1". Since each of Vcc, I2 and R1 are constants, Vout must also be a constant. See also column 6, lines 14-15.

reference completely fails to disclose the claim limitation of "generating a clock signal...." The rejection of claim 1 under §102 should accordingly be reconsidered and withdrawn.

The remarks made above in regard to claim 1 are also applicable to claim 2, which is dependent on claim 1, and to claim 31, which recites "generating a clock signal..." and therefore is also not anticipated by the Matsumoto et al. reference.

Claims 1-34 were "rejected under 35 USC §103(a) as being unpatentable" over an asserted combination of the Wissell et al. reference (U.S. Patent 6,184,736) and the Matsumoto et al. reference.

In explaining this rejection, the Examiner stated that the Wissell et al. reference "does not disclose the receiver circuit to output a single local clock signal as recited" in the claims.[2] To make up for this deficiency in the Wissell et al. reference, the Examiner proposes to incorporate teachings of the Matsumoto et al. reference into the Wissell et al. reference. Specifically, the Examiner stated that the Matsumoto et al. reference discloses in FIG. 1 thereof "a receiver circuit for producing a single clock output signal by employing both of the sinusoidal signal pair". The Examiner further stated that "[i]t would have been obvious to one skilled in the art...to incorporate the

[2] By this, Applicants understand that the Examiner recognizes that the Wissell et al. reference fails to show generating a clock signal by employing both the first sinusoidal signal and the second sinusoidal signal that make up the differential sinusoidal signal pair. Indeed, as Applicants pointed out in the Amendment filed on August 22, 2002, the receiver chip shown in FIG. 3 of the Wissell et al. reference generates respective digital clock signals from the two sinusoidal signals input to the receiver circuit.

teaching of Matsumoto into that of Wissell because a receiver circuit can be implemented in many different ways to accommodate the requirement of [a] particular application".

Applicants respectfully submit that the above rejection under §103, and the Examiner's rationale therefore, are flawed in a number of respects. First, the Matasumoto et al. reference certainly does not disclose "a receiver circuit for producing a single clock output signal". In fact, as was pointed out by Applicants in connection with the rejection of claim 1 under §102, the Matsumoto et al. reference has nothing whatsoever to do with producing a clock signal. Rather, the circuit of FIG. 1 of the Matsumoto et al. reference outputs either a video component signal or a muting signal, not a clock signal. Thus the Examiner's premise that the Matsumoto et al. reference discloses a circuit for producing a clock output signal is mistaken, and the rejection must fall on this basis taken alone.

Furthermore, the two references, Wissell et al. and Matsumoto et al., which the Examiner proposes to combine, are directed to completely different purposes. The Wissell et al. reference is concerned with clock signal distribution, whereas, as noted above, the Matsumoto et al. reference is concerned with video signal muting or mixing. A person of ordinary skill in the art who is concerned with clock signal distribution, as in the Wissell et al. reference, would have had no reason whatsoever to consider a reference such as the Matsumoto et al. reference which is concerned with video signal processing.

Moreover, the Examiner's rationale that it would have been obvious to incorporate the receiver circuit of

FIG. 1 of the Matsumoto et al. reference into the circuitry taught by the Wissell et al. reference "to accommodate the requirement of [a] particular application" is not correct, since the purpose of the receiver circuit shown in FIG. 3 of the Wissell et al. reference is to generate clock signals, whereas the function performed by the circuit of FIG. 1 of the Matsumoto et al. reference is to selectively mute a video component signal. If the circuit of FIG. 1 of the Matsumoto et al. reference were to be used to replace the circuit of FIG. 3 of the Wissell et al. reference, the Wissell et al. reference's circuitry would then cease to perform its intended function of generating clock signals, since the circuit of the Matsumoto et al. reference only outputs a video signal or a constant voltage level, and does not output a clock signal. This constitutes another reason why the proposed combination of the Wissell et al. and Matsumoto et al. references is improper.

The remarks made above in regard to the rejection of claim 1 under §103(a) are generally applicable to all of the independent claims 1, 8, 13, 22 and 31-34, since each of those claims calls for generating a clock signal by employing two sinusoidal signals of a differential sinusoidal signal pair, or by subtracting one such signal from another.

For all of the reasons stated above, it is respectfully submitted that the rejection of claims 1-34 under §103(a) should be reconsidered and withdrawn. New claims 35-42 have been added to more completely cover the invention. The new claims are respectively dependent on the independent claims 1, 8, 13, 22 and 31-34, and are therefore submitted as patentable on at least the same basis as those claims. Each of the new claims recites that a clock signal

or a local clock signal "is a square wave signal". Support for this feature is found at paragraph 24 of the present application.

For the reasons stated above, it is believed that all of the pending claims are in condition for allowance. Passage to issue is respectfully solicited.

Please charge Deposit Account No. 04-1696 in the amount of $144.00 to cover the fee for eight additional total claims in excess of those previously paid for. Applicants do not believe any other fees are due regarding this amendment. If any additional fees are required, however, please charge Deposit Account No. 04-1696. Applicants encourage the Examiner to telephone Applicants' attorney to discuss the amendment should any issues remain.

Respectfully submitted,

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VERSION MARKED TO SHOW CHANGES

In the Claims:

Claim 7 has been amended as follows:

7. (Amended) The method of claim [1] 5, further comprising applying clock gating at the local clock receivers.